CLAIMS

1. A signal processing apparatus for processing a signal using a PRML (Partial Response Maximum Likelihood) method, comprising:

an A/D converter for converting an analog signal into a digital signal;

a first waveform equalizer for amplifying a specific band of the signal to optimize data of a clock extraction system, said equalizer being connected to the A/D converter;

a second waveform equalizer for subjecting the specific band of the signal to amplification as well as waveform equalization, thereby to optimize data of a data processing system, said equalizer being connected to the A/D converter;

a timing recovery logic circuit for extracting a reproduction clock, said logic circuit being connected to the first waveform equalizer; and

a decoder for decoding data, said decoder being connected to the second waveform equalizer.

2. A signal processing apparatus comprising:

a variable gain amplifier for automatically adjusting a signal read from a recording medium so that the signal has a desired amplitude;

a filter circuit for removing a signal in a specific band, said filter circuit being connected to the variable gain

amplifier;

an A/D converter for converting an analog signal into a digital signal, said converter being connected to the filter circuit;

an adaptive transversal filter for amplifying a signal in a specific band as well as performing waveform equalization for a reproduction signal, said filter being connected to the A/D converter;

an automatic gain controller being connected to the A/D converter;

a waveform equalizer for performing waveform equalization, said equalizer being connected to the A/D converter;

a control circuit for performing baseline control, said control circuit being connected to the waveform equalizer;

a detection circuit for performing error detection and correction using a LMS (Least Mean Square) algorithm, said detection circuit being connected to the adaptive transversal filter;

a decoder for performing maximum likelihood decoding, said decoder being connected to the adaptive transversal filter; and

a timing recovery logic circuit for extracting a reproduction clock, said logic circuit being connected to the control circuit.

3. A signal processing apparatus comprising:

a variable gain amplifier for automatically adjusting a

signal read from a recording medium so that the signal has a desired amplitude;

an A/D converter for converting an analog signal into a digital signal, said converter being connected to the variable gain amplifier;

an adaptive transversal filter for amplifying a signal in a specific band as well as performing waveform equalization for a reproduction signal, said filter being connected to the A/D converter;

an automatic gain controller being connected to the A/D converter;

a waveform equalizer for performing waveform equalization, said equalizer being connected to the A/D converter;

a control circuit for performing baseline control, said control circuit being connected to the waveform equalizer;

a detection circuit for performing error detection and correction using a LMS (Least Mean Square) algorithm, said detection circuit being connected to the adaptive transversal filter;

a decoder for performing maximum likelihood decoding, said decoder being connected to the adaptive transversal filter; and

a timing recovery logic circuit for extracting a reproduction clock, said logic circuit being connected to the control circuit.

4. A signal processing apparatus as defined in Claim 2 wherein

said filer circuit is a low-pass filter which is constituted by an order equal to or lower than third order.

5. A signal processing apparatus as defined in any of Claims 1 to 3 wherein

said waveform equalizer comprises a filter having a variable tap coefficient value, and an amplification degree thereof can be set freely and minutely.

6. A signal processing apparatus as defined in Claim 1 wherein

said first waveform equalizer and said second waveform equalizer are constituted by adaptive transversal filters which subject an input signal to filter processing in accordance with an equalization coefficient.

7. A signal processing apparatus as defined in any of Claims 1 to 3 wherein

vertical resolution of the A/D converter is 7 bits or lower.

8. A signal processing apparatus as defined in any of Claims 1 to 3 wherein

said decoder is a decoding circuit using a Viterbi algorithm.

9. A signal processing apparatus as defined in Claim 3 further including

an adjustment circuit for calculating a jitter value on the basis of an output of the waveform equalizer, which output is corrected by the baseline control circuit, and automatically adjusting the degree of amplification of the waveform equalizer on the basis of the calculated jitter value.

10. A signal processing apparatus as defined in Claim 2 or 3 wherein

said recording medium is an optical disc medium.

11. A signal processing apparatus as defined in Claim 2 or 3 wherein

said recording medium is a magnetic disc medium.

12. A signal processing apparatus as defined in Claim 2 or 3 wherein

said recording medium is a semiconductor memory.

13. A signal processing method for processing a signal using a PRML (Partial Response Maximum Likelihood) method wherein

data optimization for the signal in a time axis direction and data optimization for the signal in an amplitude direction are carried out using different waveform equalizers, respectively.